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Sir: Transmitted herewith for filing is the patent application of

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For: **CHEMICAL-MECHANICAL POLISHING METHOD**

Enclosed are the following documents:

- ☒ 9 Pages of Specification
- ☒ 4 Pages of Claims
- ☒ 1 Pages of Abstract
- ☒ 4 Sheets of Drawings (Formal)
- ☒ An Assignment of the Invention to: United Microelectronics Corp.
- ☒ Recordation Cover Sheet
- ☒ Combined Declaration and Power of Attorney
- ☐ Petition to Make Special
- ☐ Declaration of Counsel
- ☐ Information Disclosure Statement and Form PTO-1449
- ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

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CHEMICAL-MECHANICAL POLISHING METHOD

CROSS-REFERENCE TO RELATED APPLICATION

5 This application claims the priority benefit of Taiwan application serial no. 87110514, filed June 30, 1998, the full disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

10 Field of Invention

 The present invention relates to a method of forming a metallic interconnect. More particularly, the present invention relates to a method of planarizing an inter-layer dielectric (ILD) layer or inter-metal dielectric (IMD) layer using a chemical-mechanical polishing (CMP) method.

15

Description of Related Art

 In the fabrication of semiconductors such as very large scale integrated (VLSI) or ultra-large scale integrated (ULSI) circuits, usually two or more metallic layers are employed to interconnect semiconductor devices in different areas of a silicon chip. In
20 general, inter-layer dielectric (ILD) or inter-metal dielectric (IMD) is used as an isolating material between metal lines in different layers. Therefore, as the design rules for forming semiconductor devices becomes highly restrictive due to miniaturization, the quality of the ILD or the IMD layer, such as its degree of surface planarity, is of growing importance.

In general, a high degree of surface planarity is an important factor in forming high-density devices using a photolithographic operation. Only a highly planar surface is capable of avoiding undesirable diffraction due to height difference during light exposure, so as to achieve a highly accurate pattern transfer. Planarization techniques can be categorized into two major groups, namely, a spin-on-glass (SOG) method and a chemical-mechanical polishing (CMP) method. However, when fabrication of semiconductors reaches the sub-half-micron stage, the spin-on-glass method is incapable of providing the degree of planarity necessary for high-quality production. Hence, the chemical-mechanical polishing method has become one of the principle means of global planarization in VLSI or ULSI production.

Figs. 1A through 1D are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to a conventional method. First, as shown in Fig. 1A, a semiconductor substrate 10 having an inter-layer dielectric (ILD) layer 12 thereon is provided. Then, a conductive line layer 14, for example, an aluminum layer or a polysilicon layer is formed over the ILD layer 12. Thereafter, an insulating layer 16 is formed by deposition over the ILD layer 12 and the conductive line layer 14. Preferably, the insulating layer 16 is formed using a high-density plasma chemical vapor deposition (HDPCVD) method. Due to the presence of the conductive lines 14 underneath, the insulating layer 16 has a pyramid-like cross-sectional profile 18 near its upper surface. In the subsequent step, an inter-metal dielectric (IMD) layer 19 is formed over the insulating layer 16.

Next, as shown in Fig. 1B, a chemical-mechanical polishing (CMP) operation is carried out to polish the IMD layer 19 so that a planar upper surface is obtained.

Because a CMP method can easily lead to the over-polishing of the surface of the IMD layer 19 or the scratching of surface by polishing particles, micro-scratches will appear on the surface of the IMD layer 19. These micro-scratches vary in size and depth, and two such scratches 20a and 20b are shown in Fig. 1B.

5 Next, as shown in Fig. 1C, conventional photolithographic and etching operations are carried out to pattern the insulating layer 16. Consequently, an opening 22 through the insulating layer 16 and the IMD layer 19 is formed. The opening 22 exposes one of the conductive line layers 14 and subsequently will serve as a via.

10 Next, as shown in Fig. 1D, a metallic layer 26 is formed over the IMD layer 19 and inside the opening 22. Thereafter, photolithographic and etching operations are again carried out to pattern the metallic layer 26, thereby forming second metallic lines 26. Due to the presence of scratches (20a and 20b) on the surface of the IMD layer 19, metal will also be deposited into the scratches forming undesirable metallic scratch lines 24a and 24b.

15 The metallic scratch lines 24a and 24b can lead to a number of defects. Fig. 2 is a top view of a conventional metallic interconnect structure. In Fig. 2, first conductive lines 30, for example, an aluminum layer or a polysilicon layer, are formed over a semiconductor substrate (not shown in the figure). In addition, second conductive lines 32 are formed above the first conductive lines 30. Through a via opening 33, the first conductive line 30 is connected to the second conductive line 32. 20 If the surface for forming the first conductive line 30 is over-polished and scratches are formed, metallic scratch lines such as the one labeled 34 in Fig. 2 will form. The metallic scratch line can form a bridge linking up neighboring second conductive lines, thereby causing short-circuiting.

In light of the foregoing, there is a need to improve the method of the chemical-mechanical polishing operation.

SUMMARY OF THE INVENTION

5 Accordingly, the present invention provides a chemical-mechanical polishing process to form a metallic interconnect that is capable of preventing the formation of micro-scratches due to over-polishing or scratching by polishing particles. Consequently, the method is capable of stopping undesirable short-circuiting or cross talks between metallic lines.

10 To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a chemical-mechanical polishing (CMP) process. The CMP process includes the steps of providing a semiconductor substrate having a first metallic line thereon, and then forming a first dielectric layer over the substrate and the first metallic line. The first
15 dielectric layer can be a silicon dioxide layer formed using a high-density plasma chemical vapor deposition (HDPCVD) method. Thereafter, a second dielectric layer is formed over the first dielectric layer. The second dielectric layer can be a silicon dioxide layer formed using a plasma-enhanced chemical vapor deposition (PECVD) method. Next, a chemical-mechanical polishing (CMP) operation is carried out to
20 polish the surface of the second dielectric layer. Subsequently, a thin cap layer is formed over the second dielectric layer, in one of several ways, including:

1. A plasma-enhanced chemical vapor deposition (PECVD) method, with silicane (SiH_4) as the main reactive agent, is used to form a silicon oxide layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

2. A chemical vapor deposition (CVD) method, with tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent, is used to form a silicon dioxide layer having a thickness of about 1000-3000Å, which can be adjusted according to the design rules.

3. A chemical vapor deposition (CVD) method, with silicane (SiH₄) as the main reactive agent, is used to form a silicon nitride layer having a thickness of about 100-3000Å, which can be adjusted according to the design rules.

4. A chemical vapor deposition (CVD) method, with silicon dichlorohydride (SiH₂Cl₂) as the main reactive agent, is used to form a silicon nitride layer having a thickness of about 100-3000Å, which can be adjusted according to the design rules.

Thereafter, a via opening is formed through the first dielectric layer, the second dielectric layer and the cap layer, wherein the opening exposes the first metallic line. Finally, a second metallic line is formed over the cap layer and fills the interior of the via opening so that the second metallic line couples electrically with the first metallic line.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Figs. 1A through 1D are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to a conventional method;

Fig. 2 is a top view showing a conventional metallic interconnect structure; and

5 Figs. 3A through 3E are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to one preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

10 Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

One major aspect of this invention is the coating of a cap layer over the dielectric layer after a chemical-mechanical polishing operation is applied to planarize the dielectric layer. Therefore, a higher degree of surface planarity can be obtained, and micro-scratches on the surface of the dielectric layer due to over-polishing or scratching by polishing particles can be eliminated. Consequently, short-circuiting between metallic lines due the presence of metallic scratch lines is prevented.

20 In general, high-density plasma chemical vapor deposition (HDPCVD) is a method that combines two basic operations. HDPCVD combines a chemical vapor deposition with an etching operation through physical bombardment by ions. High-density plasma serves to effect the ionization of reactive gases, whose kinetic energy and chemical potential is utilized to break chemical bonds and react with molecules on

the surface of the semiconductor substrate. Therefore, a layer of the reactive material is able to deposit over and fill cavities on the semiconductor substrate.

On the other hand, the etching operation in HDPCVD is dependent upon the supply of gaseous argon. Physical bombardment by argon is what causes the formation of a 45° cut at the corners of a trench. Through reactive deposition and physical etching, HDPCVD is capable of controlling the deposition of material into micro-trenches of IMD layer, and hence voids are rarely formed. Therefore, HDPCVD is particularly suitable for use in the process of forming metallic interconnect.

Figs. 3A through 3E are cross-sectional views showing the progression of manufacturing steps in producing a metallic interconnect that uses chemical-mechanical polishing according to one preferred embodiment of this invention. First, as shown in Fig. 3A, a semiconductor substrate 40 is provided. Then, an inter-layer dielectric (ILD) layer 42 is formed over the substrate 40. In the subsequent step, first metallic lines 44, for example, aluminum or polysilicon layers are formed over the ILD layer 42. The first metallic lines 44 can be formed by depositing a metallic layer using, for example, a chemical vapor deposition method or a metal sputtering method.

Thereafter, the metallic layer is patterned to form the first metallic lines. Next, an insulating layer 46 and an inter-metal dielectric (IMD) layer 50 are formed above the ILD layer 42 and the first metallic lines 44. The insulating layer 46 is formed by depositing silicon dioxide over the ILD layer 42 and the first metallic lines 44 using, for example, a high-density plasma chemical vapor deposition (HDPCVD) method.

Due to the presence of the first metallic lines 44 and the characteristic of a HDPCVD deposition, a pyramid-like cross-sectional profile 48 having a height of about

10 KÅ is formed above each first metallic line 44. The IMD layer 50 is formed by depositing silicon dioxide or F-doped silicon oxide (FSG) to a thickness of about 20KÅ over the insulating layer 46 using, for example, a plasma-enhanced chemical vapor deposition (PECVD) method.

5 Next, as shown in Fig. 3B, the surface of the IMD layer 50 is planarized, preferably by polishing using, for example, a chemical-mechanical polishing (CMP) method. Because a CMP operation can easily lead to over-polishing of the surface of the IMD layer 50 or the scratching of the surface by polishing particles, micro-scratches will appear on the surface of the IMD layer 50. These micro-scratches vary in size and
10 depth, and two such scratches labeled 52a and 52b are shown in Fig. 3B.

Next, as shown in Fig. 3C, a cap layer 54 is formed over the IMD layer 50 so that the micro-scratches 52a and 52b are covered. Hence, insulated scratches 56a and 56b are formed. The cap layer 54 preferably having a thickness of between 1000Å to 3000Å can be made from material including, for example, silicon dioxide,
15 phosphosilicate glass (PSG) or silicon-rich oxide (SRO). Moreover, the thickness of the cap layer 54 can be adjusted according to the design rule. The cap layer represents a major aspect of this invention that can be formed in several ways including: (1) using silicane (SiH_4) as the main reactive agent, a plasma-enhanced chemical vapor deposition (PECVD) method is used to form a silicon oxide layer; or (2) using tetra-ethyl-ortho-
20 silicate (TEOS) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon dioxide layer; or (3) using silicane (SiH_4) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon nitride layer; or (4) using silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent, a chemical vapor deposition (CVD) method is used to form a silicon nitride layer.

Next, as shown in Fig. 3D, conventional photolithographic and etching operations are carried out to form an opening 58 through the insulating layer 46, the IMD layer 50 and the cap layer 54. The opening 58 exposes one of the first metallic lines 44 and subsequently will serve as a via.

5 Next, as shown in Fig. 3E, metallic material, for example, tungsten or other conductive material is deposited over the cap layer and into the opening 58. Thereafter, photolithographic and etching operations are again carried out to pattern the metallic layer, thereby forming second metallic lines 60. Consequently, a metallic interconnect structure is formed.

10 In summary, the advantages of using the chemical-mechanical polishing process of this invention to fabricate metallic interconnect includes:

1. A higher quality of polished surface is obtained by eliminating micro-scratches on a polished surface due to over-polishing or scratching by polishing particles.

15 2. The polishing process used in this invention is capable of preventing the formation of metallic scratch lines, thereby eliminating possible short-circuiting pathways between subsequently formed metallic lines.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

20

WHAT IS CLAIMED IS:

1. A chemical-mechanical polishing process, comprising the steps of:
forming a first metal line layer and a dielectric layer over a semiconductor substrate;

5 polishing the dielectric layer to form a planar surface; and
 forming a thin cap layer over the dielectric layer.

2. The process of claim 1, wherein the step of forming the first metal line layer includes depositing doped polysilicon.

3. The process of claim 1, wherein the step of forming the dielectric layer
10 includes a high-density plasma chemical vapor deposition (HDPCVD) method.

4. The process of claim 1, wherein the step of forming the dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

5. The process of claim 1, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

15 6. The process of claim 1, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

7. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silicane (SiH_4) as main reactive agent such that the silicon oxide
20 layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

8. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with

tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

9. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

10. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

11. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon dioxide.

12. The process of claim 1, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

13. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

14. A method of forming a metallic interconnect, the method comprising the steps of:

- providing a semiconductor substrate having a first metallic line thereon;
- forming a first dielectric layer over the substrate and the first metallic line;
- forming a second dielectric layer over the first dielectric layer;
- polishing the surface of the second dielectric layer;
- forming a cap layer over the second dielectric layer;

forming a via opening through the first dielectric layer, the second dielectric layer and the cap layer, wherein the opening exposes the first metallic line; and

forming a second metallic line over the cap layer such that the second metallic line couples electrically with the first metallic line through the via.

5 15. The method of claim 14, wherein the step of forming the first metal line includes depositing doped polysilicon.

16. The method of claim 14, wherein the step of forming the first dielectric layer includes a high-density plasma chemical vapor deposition (HDPCVD) method.

10 17. The method of claim 14, wherein the step of forming the second dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

18. The method of claim 14, wherein the step of forming the first dielectric layer includes depositing silicon dioxide.

19. The method of claim 14, wherein the step of forming the second dielectric layer includes depositing silicon dioxide.

15 20. The method of claim 14, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

21. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silane (SiH_4) as main reactive agent such that the silicon oxide
20 layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

22. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with

tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

23. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

24. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

25. The method of claim 14, wherein the step of forming the cap layer includes depositing silicon dioxide.

26. The method of claim 14, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

27. The process of claim 14, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

ABSTRACT OF THE DISCLOSURE

A chemical-mechanical polishing process for forming a metallic interconnect includes the steps of providing a semiconductor substrate having a first metallic line thereon, and then forming a dielectric layer over the substrate and the first metallic line. Next, a chemical-mechanical polishing method is used to polish the surface of the dielectric layer. Thereafter, a thin cap layer is formed over the polished dielectric layer. The thin cap layer having a thickness of between 1000-3000Å can be, for example, a silicon dioxide layer, a phosphosilicate glass layer or a silicon-rich oxide layer. The method of forming the cap layer includes depositing silicon oxide using a chemical vapor deposition method with silicane (SiH_4) or tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent. Alternatively, the cap layer can be formed by depositing silicon nitride using a chemical vapor deposition method with silicane or silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent. Finally, a via opening is formed through the dielectric layer and the cap layer, and a second metallic line that couples electrically with the first metallic line through the via opening is formed.

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As the below named inventor, I hereby declare that:

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CHEMICAL-MECHANICAL POLISHING METHOD

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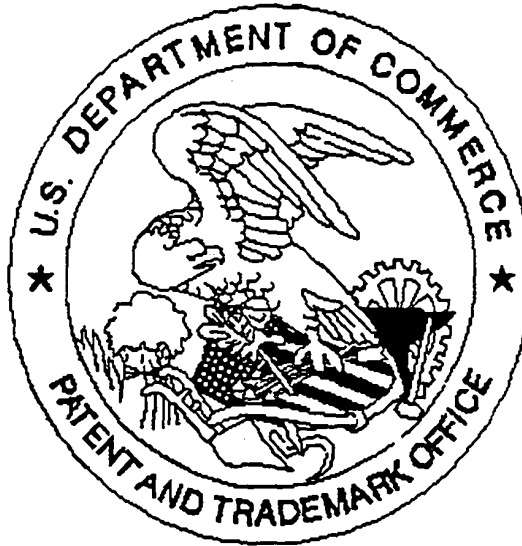
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